REMARKS

Claims 1-36 are pending in the present application. Claims 8, 19, 23, 31, and 36 were canceled and claims 1, 9, 10, 12, 20, 21, 24, 32, 33, and 35 were amended. Reconsideration of the claims is respectfully requested.

The examiner is thanked for the favor of a telephone interview on Monday, September 13, 2004. It is believed that the art arguments below correctly restate the arguments presented during the interview, during which agreement was received that these amendments overcome the cited reference.

I. 35 U.S.C. § 112, First Paragraph

The examiner has objected to claim 36 as not being enabled. This rejection is respectfully traversed. However, this claim has now been cancelled and this rejection is therefore moot.

II. 35 U.S.C. § 102, Anticipation

The examiner has rejected claims 1, 3-8, 12, 14-19, 23, 24, 26-31 and 35 under 35 U.S.C. § 102 as being anticipated by Jennings. This rejection is respectfully traversed. It is noted that the limitations of claims 8 and 19 have been incorporated into their respective independent claims.

Representative claim 1 now reads,

> 1. (Amended) A method operative in an input/output device associated with a computer system, comprising:
>
> performing, using a device having an embedded processor, a plurality of direct memory access transfers with respect to memory of the computer system, wherein parameters of the direct memory access transfers are varied pseudo-randomly;
>
> wherein the direct memory transfers are performed concurrently with memory accesses by a processor in the computer system other than said embedded processor.

Claim 1 now specifically recites that the DMA transfers are performed using a device having an embedded processor and that the transfers are performed concurrently with memory accesses by another processor. A portion of this limitation previously formed the body of claim 8; the identification of two separate processors has been added. With regard to the limitations of claim 8, the office action states,

> As in claim 8, Jennings discloses the method of claim 1, wherein the direct memory transfers are performed concurrently with memory accesses by a processor in the computer system (column 6: lines 7-38). (While the DMA controller is being configured and the direct memory transfers are being performed, the memory is accessed (column 6: lines 27-32).)[1]

The cited text from Jennings is quoted below, with the most relevant lines (27-32) being bolded in order to highlight them. Jennings states,

> Referring to FIG. 4, a schematic illustration of an exemplary random cycles test generation process for a PCMCIA DMA random cycle description generator in accordance with the present invention is shown. A random cycle description generator 38 is defined for generating random PCMCIA DMA test cycles. The PCMCIA DMA test cycles randomly generated are provided to the processor 12 by a task call 46. For this example, the processor 12 corresponds to the common cycle initiator 30 of FIG. 3. In response to the task call 46 from the PCMCIA DMA random cycle description generator 38, the processor 12 provides a bus cycle 48 to configure a DMA controller 14. When the PCMCIA DMA random cycle description generator 38 detects that it owns the bus of the processor 12, the PCMCIA DMA random cycle description generator 38 provides a task call 50 to call a PCMCIA DMA driver 42. In response to the call by the PCMCIA DMA random cycle description generator 38, the PCMCIA DMA driver 42 either provides data to or fetches data from a PCMCIA controller 43 across a PCMCIA DMA bus 44. The PCMCIA controller 43 is coupled to a memory controller 41. **Data is transferred between the PCMCIA controller 43 and the memory controller 41, the direction of data transfer depending on the type of DMA test cycle. The memory controller 41 provides or receives data from a memory 40 across a memory bus 47. The memory 40 is one exemplary block of the design under test 10.**

It is submitted that Jennings is discussing a DMA data transfer, which requires the use of a processor. However, the advantage of a DMA transfer is that the processor used is not the main system processor, but an embedded processor on the device performing the DMA transfer. The claim has now been amended to recite that these two separate processors – the embedded processor performing the DMA transfer and another processor (such as the main processor) – are actively accessing the memory at the same time. Jennings does not showing this further limitation. Therefore, this rejection under 102 has been overcome.

Furthermore, Jennings does not teach, suggest, or give any incentive to make the needed changes to reach the presently claimed invention. Absent some teaching to have another processor accessing the memory at the same time as the DMA access, one of ordinary skill in the art would not be led to modify Jennings to reach the present invention when the reference is examined as a whole. Absent some teaching, suggestion,

[1] Office action of 6/17/2004

or incentive to modify Jennings in this manner, the presently claimed invention can be reached only through an improper use of hindsight using the applicants' disclosure as a template to make the necessary changes to reach the claimed invention.

III. Objection to Claims

The examiner has stated that claims 9, 10, 20, 21, 32, and 33 were objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In response, claims 9, 20 have been rewritten to overcome this objection; the limitations of claim 32 were added to its independent claim, and the dependencies of claims 10, 21, and 33 have been changed to make them dependent on allowable claims.

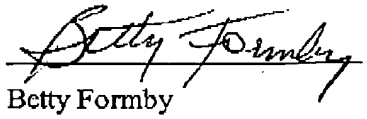
IV. Conclusion

It is respectfully urged that the subject application is patentable over Jennings and is now in condition for allowance.

The examiner is invited to call the undersigned at the below-listed telephone number if in the opinion of the examiner such a telephone conference would expedite or aid the prosecution and examination of this application.

DATE: September 17, 2004

Respectfully submitted,



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